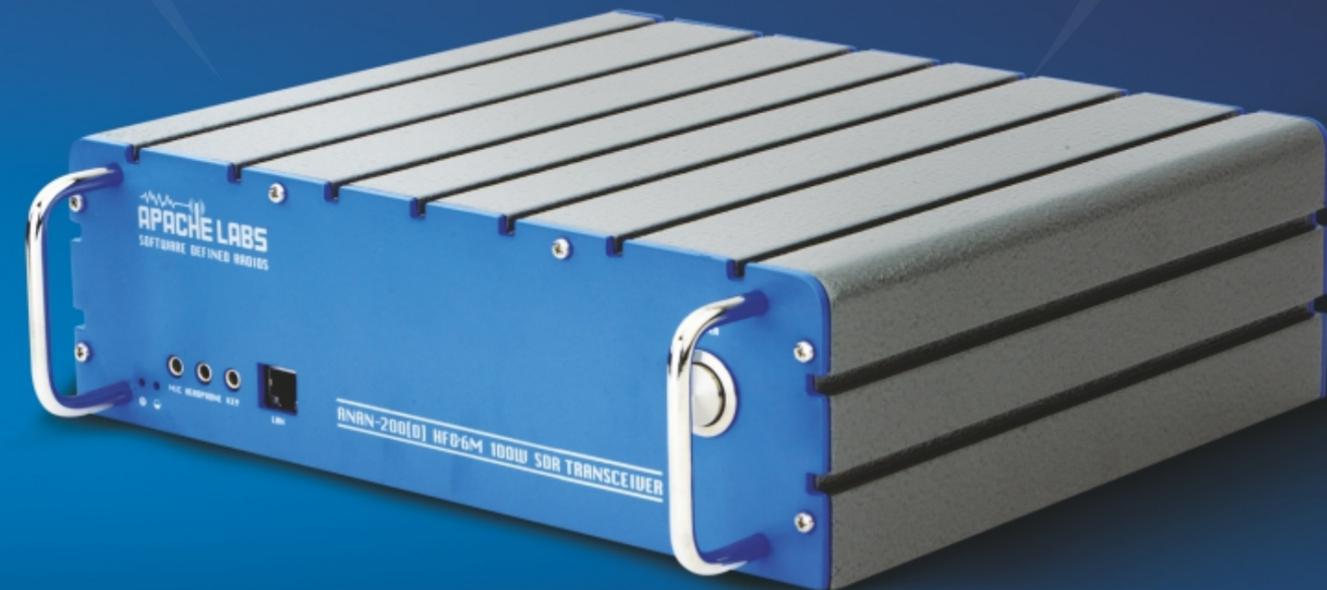


SPECIFICATIONS & HIGHLIGHTS

	ANAN-10	ANAN-100	ANAN-100D	ANAN-200D
Pricing	US\$ 1679.00	US\$ 2489.00	US\$3489	US\$4289
Warranty	2Year Limited Manufacturer's Warranty*			
FPGA	EP3C40	EP3C40	EP4CE115	EP4CGX150
Logic Elements	40K	40K	115K	150K
On Board DSP Processing Capability	Yes (limited by FPGA LEs)	Yes (limited by FPGA LEs)	Extensive, including optional Soft Core	Extensive, including optional Soft Core
FLASH RAM	16MB	16MB	128MB	128MB
SRAM	-	-	32Mbit	32Mbit
Master Clock	122.88MHz	122.88MHz	122.88MHz	122.88MHz
CLOCK Phase Noise @ 10KHz	-149dBc	-149dBc	-149dBc	-149dBc
10MHz Reference TCXO	± 2.5PPM	± 0.1PPM	± 0.1PPM	± 0.1PPM
External 10MHz Reference Input	Yes	Yes	Yes	Yes
Ethernet	GIGABIT	GIGABIT	GIGABIT	GIGABIT
Modes	AM,FM,RTTY,CW,LSB,USB, DIGITAL (limited only by the application software)			
Frequency Step	1 Hz	1 Hz	1 Hz	1 Hz
Antenna Ports(50 Ω)	3	3	3+1	3+1
I/O's	Seven User-Configurable Open-collector outputs Four user- configurable 12 bit buffered Analogue inputs	Seven User-Configurable Open-collector outputs Four user- configurable 12 bit buffered Analogue inputs	Seven User-Configurable Open-collector outputs Four user- configurable 12 bit buffered Analogue inputs	Seven User-Configurable Open-collector outputs Four user- configurable 12 bit buffered Analogue inputs
VNA	10Khz - 55Mhz VNA	10Khz - 55Mhz VNA	10Khz - 55Mhz VNA	10Khz - 55Mhz VNA
Housing	Extruded Aluminum Rugged Housing	Customized Rugged Rack Mount Style Housing	Customized Rugged Rack Mount Style Housing	Customized Rugged Rack Mount Style Housing
Dimensions(W×D×H)	135mm ×160mm ×68mm	448mm ×242mm ×88mm	448mm ×242mm ×88mm	448mm ×242mm ×88mm
Weight	1.5Kg (Approx)	4.5Kg (Approx)	4.5Kg (Approx)	4.5Kg (Approx)
RECEIVER				
Architecture	Direct Down Conversion	Direct Down Conversion	Direct Down Conversion	Direct Down Conversion
Number of ADC'S	1	1	2	2
Number of Receivers**	4	4	7	7
ADC Resolution	16 BIT	16 BIT	16 BIT	16 BIT
Frequency Coverage	10 KHz- 55 MHz			
Dynamic Range	125 dBm	125dBm	125dBm	125dBm
Diversity Reception	No	No	Yes	Yes
MDS @ 14.2MHz (500Hz Bandwidth)	-138 dBm	-138 dBm	-138 dBm	-138 dBm
Preamplifier	20 dB	20dB + LNA for 6M	20dB + LNA for 6M	20dB + LNA for 6M
Attenuator	Software selectable 31dB in 1dB steps			
Spurious and Image rejection	Greater than 100 dB			
Audio Amplifier	1W @ 8Ω	1W @ 8Ω	1W @ 8Ω	1W @ 8Ω
TRANSMITTER				
Architecture	Direct Up Conversion	Direct Up Conversion	Direct Up Conversion	Direct Up Conversion
Number of DAC'S	1	1	1	1
RF Output	1-10W	1-100W	1-100W	1-100W
Coverage	160M-6M	160M-6M	160M-6M	160M-6M
Modes	AM,FM,RTTY,CW,LSB,USB, DIGITAL (limited only by the application software)			
Modulation	Digital Low Level	Digital Low Level	Digital Low Level	Digital Low Level
Carrier & Unwanted Sideband Suppression	Greater than -90dbc	Greater than -90dbc	Greater than -90dbc	Greater than -90dbc
Harmonic Suppression	Greater than 50dB(HF) Greater than 60dB(VHF)			
IMD3 @ 100W PEP With Adaptive Predistortion enabled	Better than -45dB on all Bands (160M - 6M)	Better than -45dB on all Bands (160M - 6M)	Better than -45dB on all Bands (160M - 6M)	Better than -45dB on all Bands (160M - 6M)

Specifications subject to change, copyright 2014 - Apache Labs Pvt Ltd.

* Apache Labs Warranty Conditions apply
** Number of concurrent receivers is also dependent on the PC SDR Software used



APACHE LABS ANAN SDRs



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Sector - 49, Sohna Road, Gurgaon - 122001, Haryana, India
Tel: 91-0124-4245173/4/5 (10AM - 6PM IST) Email: support@apache-labs.com

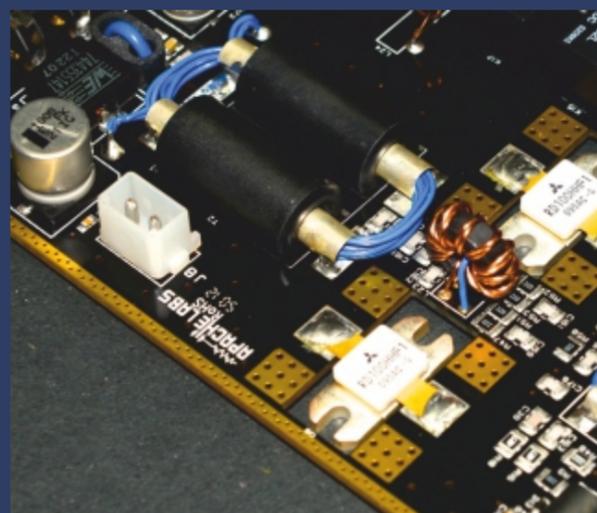
www.apache-labs.com

AN INTRODUCTION

The ANAN radios define a new level of performance in Amateur Radio transceivers, based on the very popular OpenHPSDR designs, they represent the state-of-the-art in the amateur HF radio space.



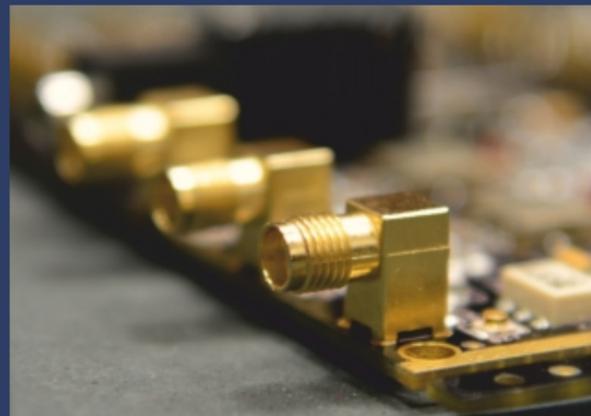
The ANAN-100D/200D have true phase coherent dual front end comprising of two 16 bit 130MSPS ADCs and a large Cyclone IV FPGA which allows for a huge amount of headroom and DSP processing power, the current firmware incorporating 14 receivers and diversity reception uses around 30% of the FPGA resources!



The ANANs use rugged Mosfets for the 100W Power Amplifier, our PA design uses custom input/output transformers designed for an almost flat gain response from 160M through 6M, unlike other radios the IMD is -45dB (with Pure Signal enabled on all bands) below PEP even on

6M, the entire housing is a single piece aluminium extrusion and heat sink for the PA, resulting in very effective cooling and minimal fan noise.

The ANAN radios use gold plated connectors for all RF connections resulting in improved performance and increased dependability.



DEVELOPMENT TEAM

The ANAN SDRs are based on the work of the OpenHPSDR community, the development of these groundbreaking SDRs is an example of cross continental team work.

Joe Martin, K5SO
Conceptualization of the Angelia & Orion SDRs, Firmware & beta testing

Doug Wigley, W5WC
PC software development, integration & beta testing

Phil Harman, VK6PH
Hardware Design, Verilog code & beta testing

Abhishek Prakash
Hermes, Angelia and Orion Hardware design, PCB layout and beta testing

Warren C Pratt, NR0V
Developer of WDSP and PureSignal (Adaptive Predistortion Algorithm), the DSP Processing core used in the Orion SDR

Kjell Karlsen, LA2NI
RF Amplifiers, SMPS and hardware design

Kevin Wheatley, M0KHZ
Hermes Design conceptualization

Dr. Hermann von Hasseln, DL3HVH
Developer of cuSDR

WITH APPROPRIATE SOFTWARE AND ANTENNAS OUR SDRS CAN BE USED FOR :

- HF direction finding
- Rx beam steering using a fixed array of antennas
- Phil Harman, VK6PH's VNA Application
- Alex, VE3NEA's VNA Application
- Polarization diversity operations (using two of the ADCs) to remove Faraday Rotation effects and to remove polarization misalignment effects during Rx
- Spatial diversity operations to mitigate/reduce signal fading compared with single antenna operations

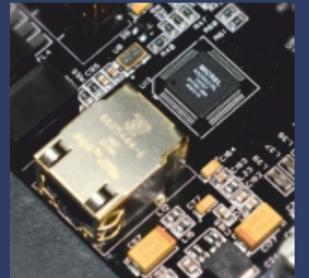
BUILT IN A RUGGED SINGLE PIECE ALUMINUM EXTRUDED SECTION



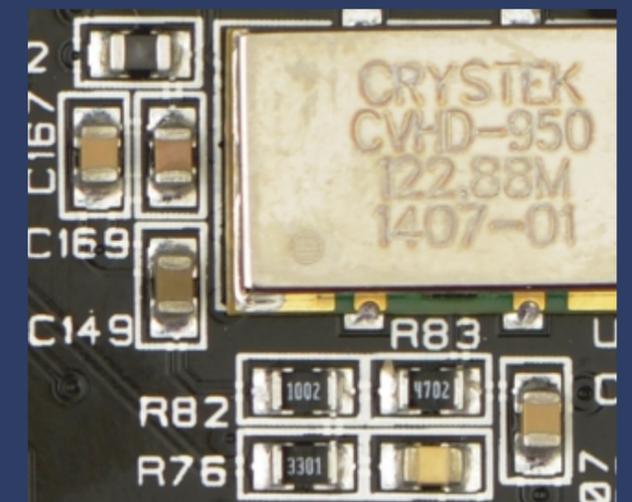
Highly integrated 8 layer design, use of state-of-the-art FPGAs enables huge DSP processing capability and logic implementation.

Ethernet Interface to the PC allows for an IP enabled networked SDR Transceiver.

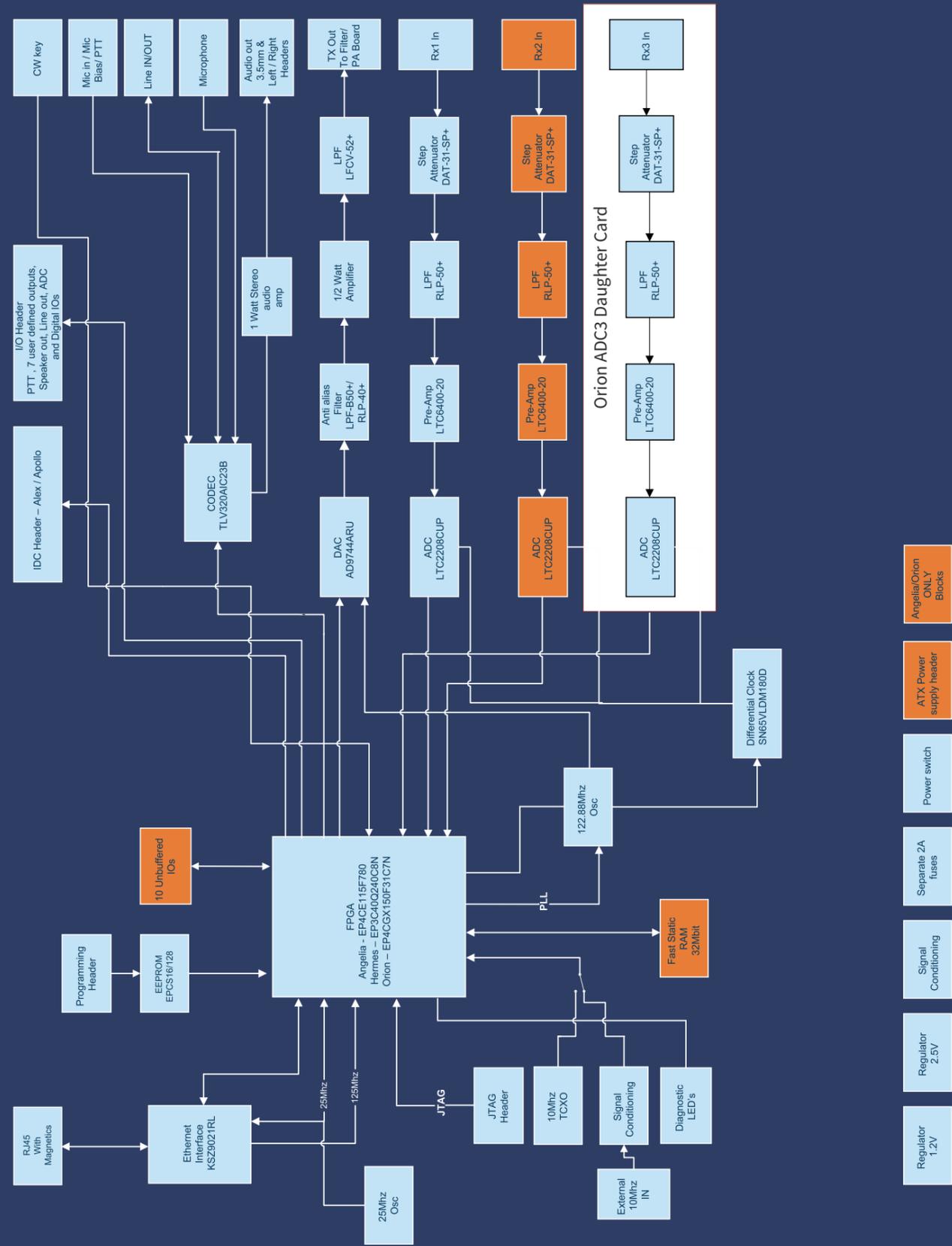
All ANAN transceivers use a Gigabit Ethernet interface to connect to the outside world, this means no drivers, huge bandwidth, better noise isolation from the PC and networked radios with remote access and much more. The PC to SDR cable can be longer or you can go wireless and connect the radio to your Wi-Fi and use the radio from anywhere in your home or office.



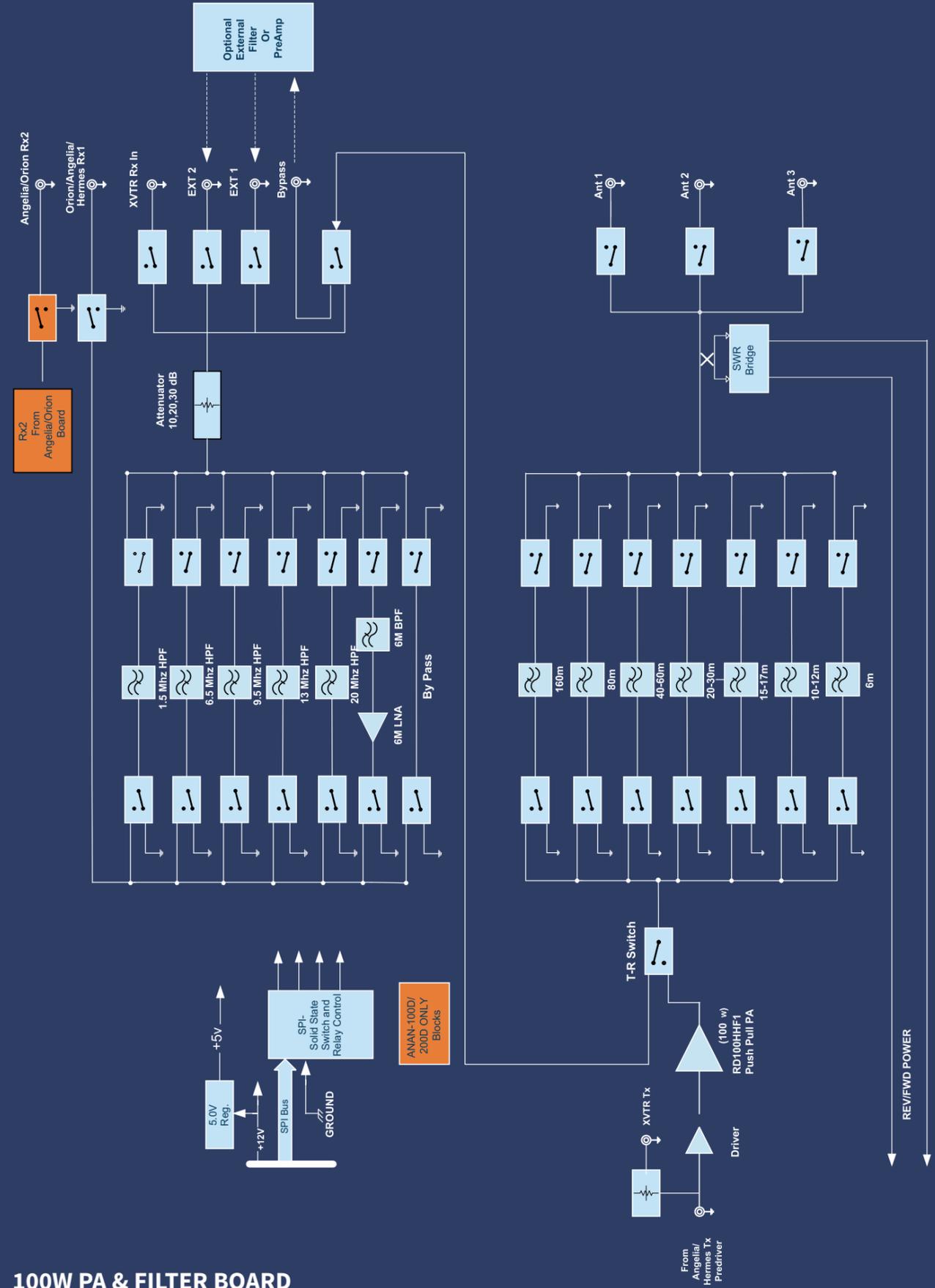
Unlike conventional radios where front end filtering is at the cost of degraded receiver IMD due to the small BPF inductors and less than optimum filter shape factor (low Q circuits) the ANAN-100/100D/200D use a combination of LPF/HPF banks with oversized toroids to achieve excellent BPF shape factor without effecting the IMD of the receiver.



With a blocking dynamic range of over 120dB which is independent of signal spacing the limiting factor could be the LO phase noise, keeping this in mind the designers have used an extremely low noise VCXO, when phase locked with the 10MHz TCXO the phase noise at 200Hz is <-130dB/Hz



ORION/ANGELIA/HERMES BLOCK DIAGRAM

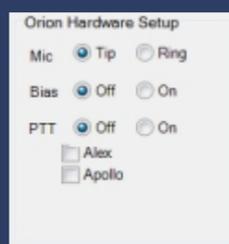


100W PA & FILTER BOARD

ANAN-200D AN INTRODUCTION



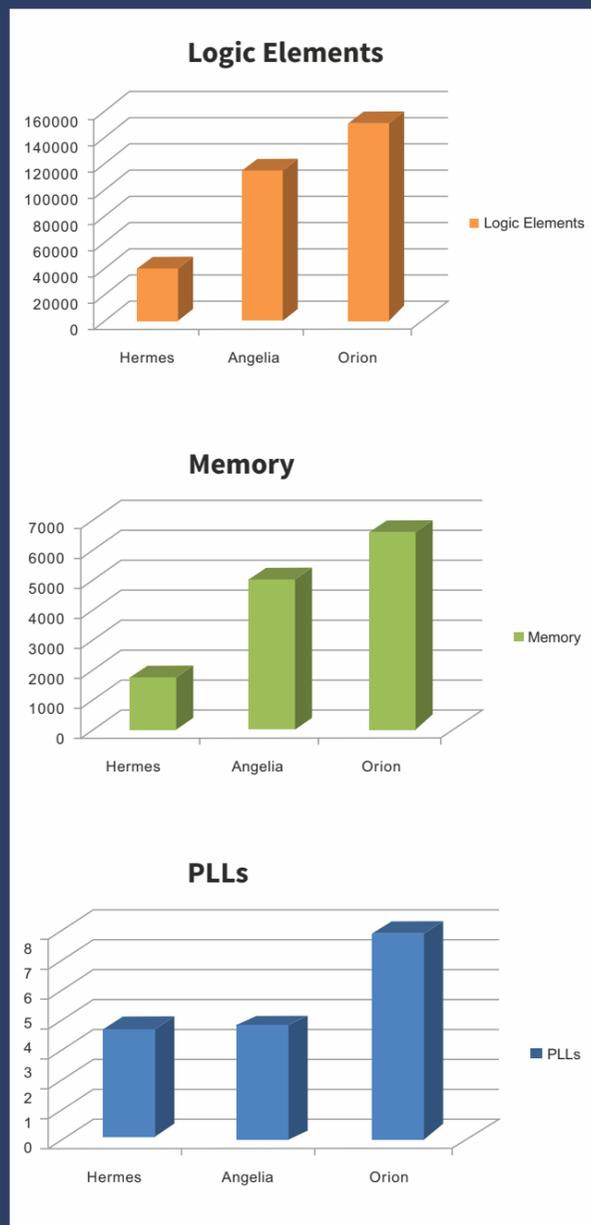
The ANAN-200D Software Defined Radio is The most powerful Amateur Radio Transceiver building available today, it builds on the very successful OpenHPSDR Hermes and the Apache Labs ANAN-100/100D designs and offers unprecedented performance/functionality not available in any other HF/6M radio transceiver.



All major controls and settings such as PTT/Mic/Bias/External reference switching is under software control or automated, hence this is an ideal platform for those

who would like a consumer plug & play SDR solution.

The ANAN-200D has been designed keeping in mind advanced applications and uses the largest FPGA in any commercially available Amateur Radio SDR, the current implementation uses less than 35% of the resources and has more than adequate headroom for the future applications.



FPGA RESOURCE COMPARISON

ANAN-10/100 - Uses Hermes

ANAN-100D - Uses Angelia

ANAN-200D - Uses Orion

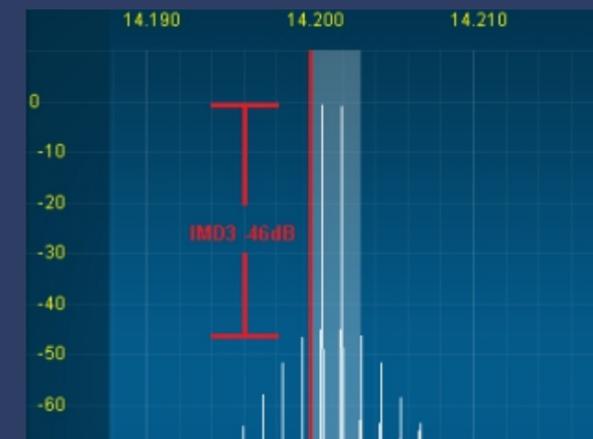
The quest for a clean transmitter requires one to either operate in very inefficient Class A mode (at reduced efficiency and power outputs) or invest in a 50v Mosfet design which provides a 10dB improvement in IMD in the best case scenario.

The ANANs has been designed from the ground up to use modern digital predistortion algorithms to mitigate and reduce the IMD created in the transmitter, 50dB IMD3 has been achieved using Warren's (NR0V) revolutionary new WDSP engine which implements adaptive predistortion.

Implementation of predistortion requires that 40Khz transmit and receive bandwidths be flat within 0.01dB, this amazing feat has been implemented in the FPGA firmware by Phil, VK6PH.

WDSP is currently embedded into PowerSDR™, cuSDR and the HPSDR android application.

Exceptional transmitter output linearity has been achieved, the results are astounding and far superior to any other Amateur radio transceiver available in the market today, these improvements are also available to the Hermes and Angelia based SDRs, the image on the right depicts the IMD @ 100W on the ANAN-200D.



cuSDR operating with four independent receivers plus 0 - 55MHz display

THE ANAN SDRs WILL WORK ON A MULTITUDE OF SOFTWARE PLATFORMS SUCH AS :

- The OpenHPSDR flavours of PowerSDR™
- cuSDR
- Kiss Konsole
- GNURADIO- OpenHPSDR
- John Melton's (G0ORX/N6LYT) android application for The OpenHPSDR hardware
- GHP3DR3, GHP3DR3-QT